

ABSTRACT OF THE INVENTION

FULL MULTIPROCESSOR SPECULATION MECHANISM IN A SYMMETRIC
MULTIPROCESSOR (SMP) SYSTEM

5 Described is a data processing system and processor
that provides full multiprocessor speculation by which
all instructions subsequent to barrier operations in a
instruction sequence are speculatively executed before
10 the barrier operation completes on the system bus. The
processor comprises a load/store unit (LSU) with a
barrier operation (BOP) controller that permits load
instructions subsequent to syncs in an instruction
sequence to be speculatively issued by the LRQ prior to
15 the return of the sync acknowledgment. Load data
returned by the speculative load request is immediately
forwarded to the processor's execution units for
speculative execution with subsequent instructions. The
returned data and results of subsequent operations are
20 held temporarily in the rename registers. A
multiprocessor speculation flag is set in the
corresponding rename registers to indicate that the value
is "barrier" speculative. When a barrier acknowledge is
received by the BOP controller, the BOP controller
25 messages logic affiliated with the processor's registers,
which then resets the flag(s) of the corresponding rename
register(s).